SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device including a transistor and a diode and to a manufacturing method of the same.

BACKGROUND ART

[0002] Heretofore, as this type of technology, for example, one described in a literature shown below has been known (refer to Patent Literature: Japanese Patent Laid-Open Publication No. 2005-183563). This literature describes a technology of a semiconductor device including: a trench-type transistor in which a gate electrode is embedded in a trench; and a diode in which a hetero semiconductor region is used as an anode and a drift region is used as a cathode. The hetero semiconductor region that composes the anode of the diode is arranged along such gate electrodes, which are adjacent to each other, at a predetermined interval therewith so as to be sandwiched between the gate electrodes concerned.

SUMMARY OF INVENTION

[0003] In the above-described conventional semiconductor device, the hetero semiconductor region is arranged and formed in a plane direction of a semiconductor substrate with respect to the gate electrodes so as to be adjacent to the gate electrodes. That is to say, a region in which the hetero semiconductor region is to be formed has been required in the plane direction of the semiconductor substrate. As a result, area efficiency of an element in the semiconductor substrate has been poor, and this has been hindrance in the event of enhancing an integration degree.

[0004] In this connection, the present invention has been made in consideration of the foregoing problem. It is an object of the resent invention to provide a semiconductor device in which the integration degree is enhanced by increasing the area efficiency, and to provide a manufacturing method of the same.

[0005] In order to solve the foregoing problem, the present invention is characterized in that an anode region is formed on a bottom portion of a trench in which a gate electrode is formed or in a drift region immediately under the trench, that a contact hole is formed in the trench at a depth reaching the anode region, that a source electrode is embedded in the contact hole while interposing an inner wall insulating film therebetween, and that the anode region and the source electrode are electrically connected to each other in a state of being insulated from the gate electrode by the inner wall insulating film.

BRIEF DESCRIPTION OF DRAWINGS

[0006] FIG. **1** is a cross-sectional view showing a configuration of a semiconductor device according to Embodiment 1 of the present invention.

[0007] FIG. **2**A is a process cross-sectional view showing a manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0008] FIG. **2**B is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0009] FIG. **2**C is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0010] FIG. **2**D is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0011] FIG. **2**E is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0012] FIG. **2**F is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0013] FIG. **2**G is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0014] FIG. **2**H is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0015] FIG. **2**I is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0016] FIG. **2**J is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 1 of the present invention.

[0017] FIG. **3** is a cross-sectional view showing a configuration of a semiconductor device according to Embodiment 2 of the present invention.

[0018] FIG. **4**A is a process cross-sectional view showing a manufacturing method of the semiconductor device according to Embodiment 2 of the present invention.

[0019] FIG. **4**B is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 2 of the present invention.

[0020] FIG. **4**C is a process cross-sectional view showing the manufacturing method of the semiconductor device according to Embodiment 2 of the present invention.

[0021] FIG. **5** is a plan view showing a configuration of a semiconductor device according to Embodiment 3 of the present invention.

[0022] FIG. **6** is a plan view showing another configuration of the semiconductor device according to Embodiment 3 of the present invention.

[0023] FIG. **7** is a plan view showing another configuration of the semiconductor device according to Embodiment 3 of the present invention.

[0024] FIG. **8** is a plan view showing another configuration of the semiconductor device according to Embodiment 3 of the present invention.

[0025] FIG. **9** is a plan view showing a configuration of a semiconductor device according to Embodiment 4 of the present invention.

[0026] FIG. **10** is a plan view showing another configuration of the semiconductor device according to Embodiment 4 of the present invention.

[0027] FIG. **11** is a plan view showing another configuration of the semiconductor device according to Embodiment 4 of the present invention.

DESCRIPTION OF EMBODIMENTS

[0028] By using the drawings, a description is made below of embodiments for carrying out the present invention.